DESIGN GUIDE EMBEDDING TECHNOLOGY
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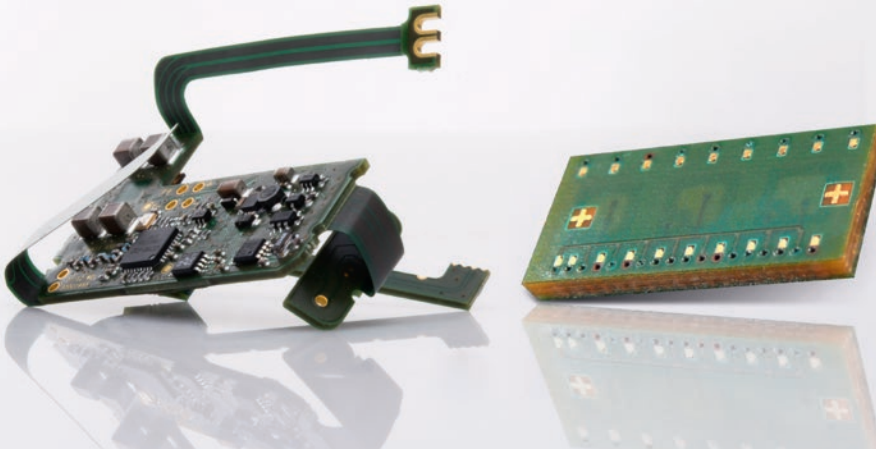
WÜRTH ELEKTRONIK

Embedding Technology

Design Guide



Embedding Technology

The future of electronics is tending towards higher reliability, more functionality and increasing miniaturisation. The efficient use of ever smaller housing volumes and tiny surfaces is gaining in importance. ET (Embedding Technology) serves as a solution for reduced spaces.

In an embedding process, active or passive components are positioned in the stack up so that they are completely integrated into its construction. Würth Elektronik distinguishes between three manufacturing processes: ET Solder, ET Microvia and ET Flip-Chip.

The fields of application range from the automotive industry to industrial electronics to medical technology and to sensor technology.

Below is an overview on the subject of "Embedding Technology" and practical tips for design:

- Indicators for the choice of technology
- Technology comparison
- Availability of components
- Design Rules

The advantages of Embedding Technology at a glance:

Miniaturisation

- Housing replacement
- Saving of assembly space on the exterior PCB layers

Function

- Integrated shielding
- Short signal paths
- Protection against plagiarism

Reliability

- Protection against environmental influences
- Fully encapsulated and supported components
- Thermal management

Indicators for technology use

ET Solder

- Active components that are not available as a bare die
- Active and passive components
- Range of the solid SMD components can be used (with restrictions)

ET Microvia

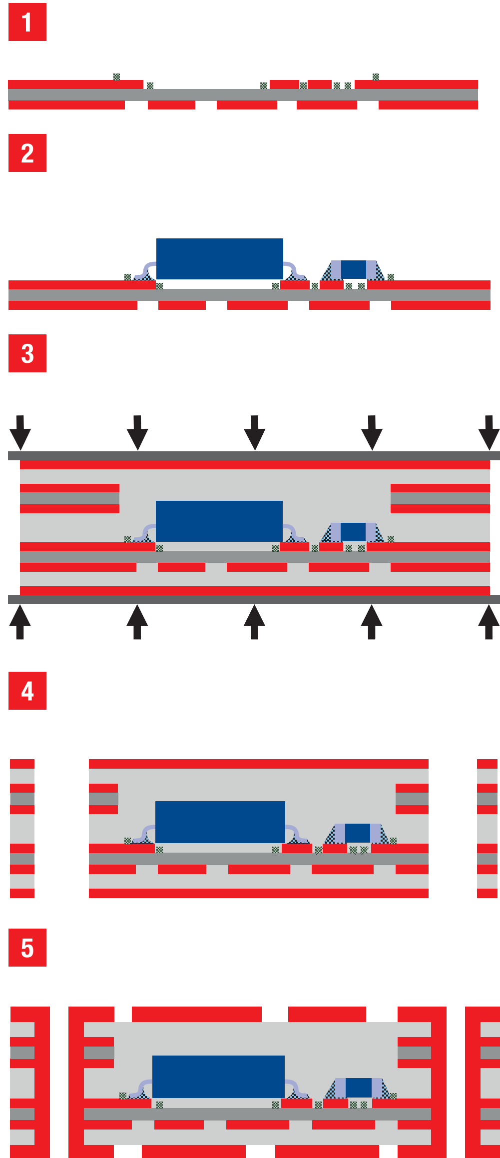
- Combination of active and passive components
- Highly reliable assembly and packaging technology
- Copper or nickel-palladium pad metallisation on the components

ET Flip-Chip

- Active components, which were previously wire-bonded
- No passive components possible
- Active components with pitch < 250 µm

Process Flows

ET Solder



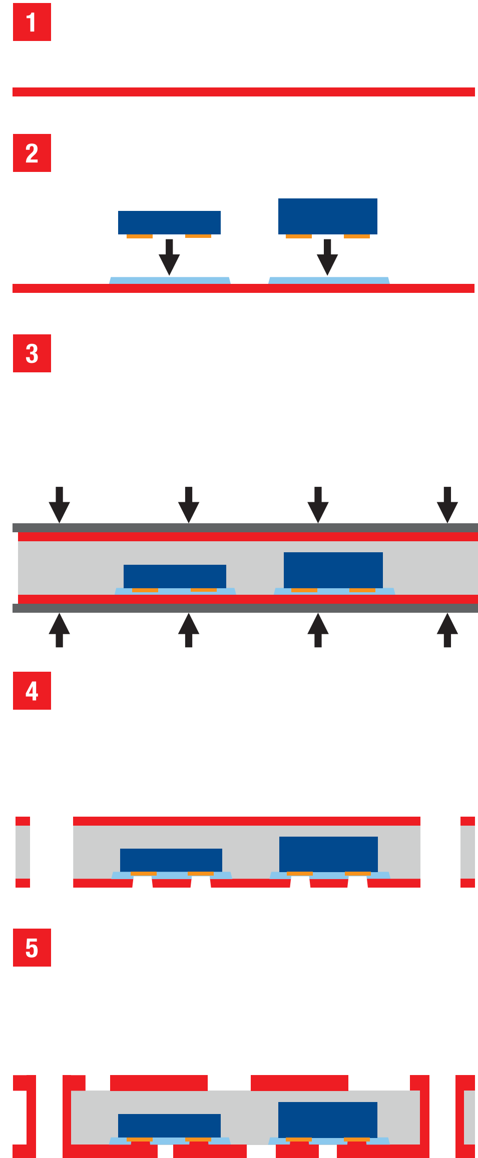
1 Structured inner layer core with footprint for SMD components

2 SMD assembly (lead free reflow)

3 Multilayer lamination

4+5 Depending on customer request, additional circuit board processes

ET Microvia Version 1



1 Cu foil as starting substrate

2 Assembly (face-down) on Cu foil with non-conductive adhesive (NCA)

3 Multilayer lamination

4 Laser drilling in Cu and adhesive

5 Electrical connection between chip and PCB via Cu metallisation and structuring

The process flows shown here only serve as a description of the process. The actual stack-up and the number of layers will be adapted to the customer´s requirement.

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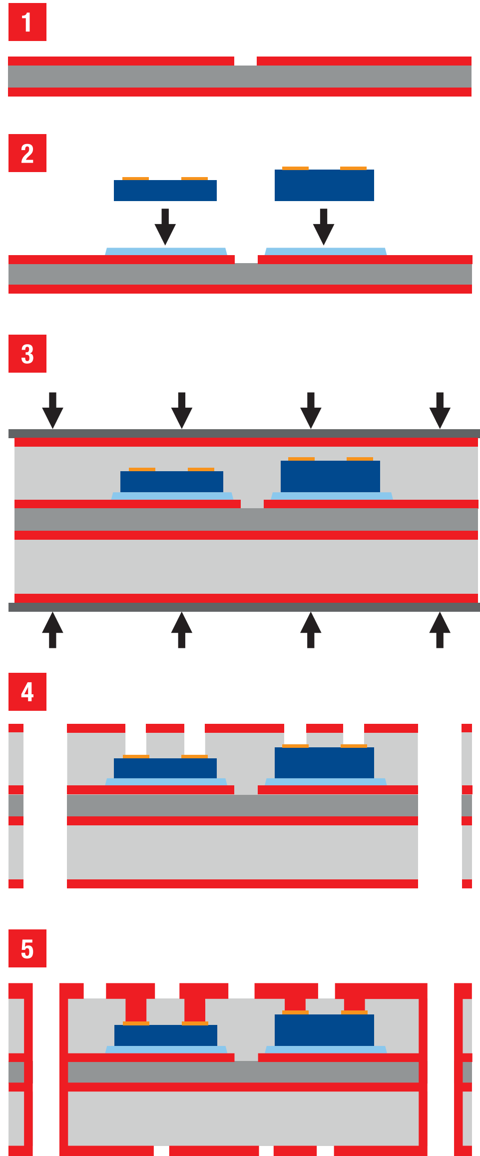
Process Flows

ET Microvia Version 2



1 Structured inner layer core

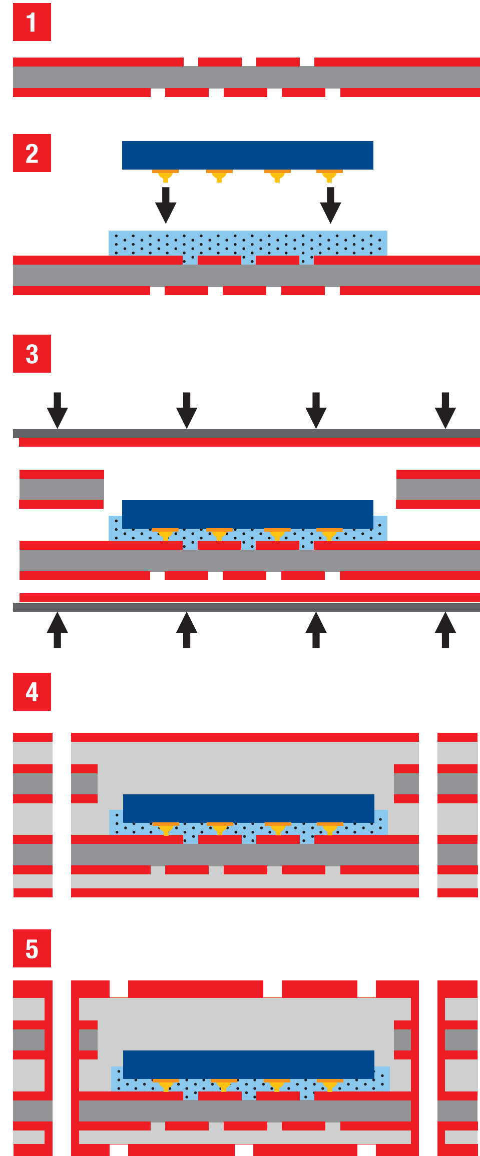
2 Assembly (face-up) on core with conductive (ICA – isotropic conductive adhesive) or non-conductive adhesive (NCA)

3 Multilayer lamination

4 Laser drilling in Cu and resin

5 Electrical connection between chip and PCB via Cu metallisation and structuring

ET Flip-Chip



1 Structured inner layer core with footprint for Flip-Chip

2 Flip-Chip assembly using ACA adhesive (anisotropic conductive adhesive)

3 Multilayer lamination

4+5 Depending on customer request, additional circuit board processes

The process flows shown here only serve as a description of the process. The actual stack-up and the number of layers will be adapted to the customer´s requirement.

Project planning and layout tips

Process for new projects

The following data and documents are required for initial implementation of projects with embedded components:

BOM (bill of materials) of the components that are to be embedded (not the BOM for the outer layer)
- Including all mechanical dimensions for calculating the volume of the required installation space
- Including all mechanical dimension tolerances

Data records (preference is given to Extended Gerber or ODB++) and documents with
- PCB outline (including delivery panel outline, if necessary)
- Planned/required assembly design of the inner layer (including the dimensions for contacts, such as gull-wing and J leads), as well as the associated pick & place data (if available)
- Layout data (if already available)
- Required number of layers and required layer connections, and the necessary copper layer thicknesses
- Necessary, predefined spacing between layers (e.g. for impedances or sections of insulation)

Availability and requirements for the components

ET Solder

All SMD components can be used in principle with the following restrictions:
- Minimum design size EIA 0201
- Maximum design size 5x5 mm² (further sizes may be available on request)
- Maximum component thickness dependent upon the layer structure
- No liquids or electrolytes permitted in the component
- No air pockets permitted in the component, such as with quartz crystals with metallic cover, for example

ET Microvia

Passive components:
- Passive components (capacitors and resistors) with copper termination are purchased from Würth Elektronik directly.
- Designs: EIA 0402 and, in some cases, EIA 0201
- Resistance values: E96 series
- Capacitor values: Please enquire, as only a few values are available from the manufacturers

Active components:
- Bare dies with Cu-pad metallisation
- Bare dies with NiPd metallisation

ET Flip-Chip

No passive components possible

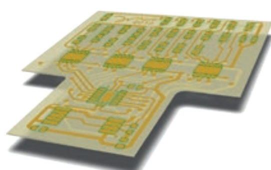
Active components:
- Bare dies with wire-bonded Au stud bumps
- Bare dies with Au stud bumps fitted at wafer level

Layout tips

ET Solder

Virtually all EDA tools are unable to show any solder resist frames on inner layers.

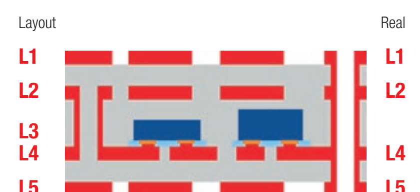
→ Solder resist frames for internal layers can be defined on a mechanical layer.



ET Microvia

In most cases, it has previously not been possible to define a microvia between the component and copper layer.

→ Can be achieved by adding a (virtual) copper layer.



Design Rules

Unless agreed to the contrary, the IPC-7092 applies to all products with embedded components. The associated PCB production complies with IPC-A-600 class II and IPC-A-610 class II assemblies.

Depending on the final buildup and design of the circuit board with embedded components, all circuit board designs with embedded components are subject to the Design Rules/Design Guides “Basic Design Guide”, “Flex-Rigid Design Guide”, “Thermal Management Design Guide” and “HDI Design Guide” that are currently applicable at Würth Elektronik. The additional specific design rules are as follows:

ET Solder

Regarding ET Solder, the design rules are only extended to include the rules for the inner solder mask which may NOT be designed across the entire area. The solder resist function is defined by frames surrounding the solder pads.

This rule for the solder mask applies to Cu thicknesses of 18 µm and 35 µm on the inner layer to be assembled. Please contact us for other Cu thicknesses.

ET Microvia

These minimum dimensions shown for Cu tracks, microvias and pads for the microvia only apply to the layer to be assembled. The maximum Cu thickness of this layer is 25 µm. Please contact us for other Cu thicknesses.

ET Flip-Chip

The dimensions for the Cu tracks for the ET Flip-Chip are based on Cu thicknesses $\leq$ 18 µm. Please contact us for Cu thicknesses $>$ 18 µm.

Component positioning – resin flow

The following applies to the cut-outs milled in prepreg: All points within the cut-out must be accessible at a distance of $\leq$ 5.0 mm from the boundary of the cut-out.

! For further information on the subject of embedding please visit our website at www.we-online.com/embedding